

What is claimed is:

- 1 1. A semiconductor device comprising:  
2 a plurality of first bump electrodes arranged on a main surface,  
3 and each of said plurality of first bump receiving signals or  
4 power;  
5 a plurality of dummy bump electrodes arranged on said main  
6 surface, and each of said plurality of dummy bump electrically  
7 connected to associated one of said plurality of first bump  
8 electrodes.
- 1 2. The semiconductor device as claimed in claim 1 further  
2 comprising:  
3 a plurality of protection circuit electrically coupled to  
4 said plurality of first bump electrodes.
- 1 3. The semiconductor device as claimed in claim 1, further  
2 comprising:  
3 a plurality of test electrodes electrically connected to said  
4 first bump electrodes.
- 1 4. The semiconductor device as claimed in claim 3, wherein  
2 said plurality of test electrodes being arranged along four  
3 edges of said semiconductor device.
- 1 5. The semiconductor device as claimed in claim 1, wherein said  
2 plurality of dummy bump electrodes being higher than said  
3 plurality of chip electrodes.
- 1 6. The semiconductor device as claimed in claim 1, wherein said

2 plurality of dummy bump electrodes being arranged closer than  
3 said plurality of first bump electrodes.

1 7. The semiconductor device as claimed in claim 1, wherein said  
2 plurality of dummy bump electrodes being arranged between said  
3 plurality of first bump electrodes and said plurality of said  
4 chip electrodes.

1 8. The semiconductor device as claimed in claim 1, wherein said  
2 plurality of dummy bump electrodes being provided for relaxation  
3 of stress at mounting said semiconductor device.

1 9. The semiconductor device as claimed in claim 1, wherein said  
2 plurality of dummy bump electrodes and said plurality of first  
3 bump electrodes being arranged alternately along to  
4 circumference of bump group.

1 10. A semiconductor device comprising:  
2 a semiconductor substrate;  
3 an insulating layer formed above said semiconductor  
4 substrate;  
5 a plurality of first bump electrodes formed on said insulating  
6 layer, and each electrically connected to associated one of  
7 plurality elements formed in said semiconductor substrate; and  
8 a plurality of second bump electrodes formed on said insulating  
9 layer, and each electrically connected to associated one of said  
10 plurality of first bump electrodes.

1 11. The semiconductor device as claimed in claim 10, further

2 comprising:

3 a plurality of test pad formed on said insulating layer, and  
4 each electrically connected to at least associated one of  
5 plurality of first bump electrodes.